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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

| EXAMINER |
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WELLS, KENNETH B

| ART UNIT | PAPER NUMBER |
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2816

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/649,261

Applicant(s)

DAVIS, JEFFREY B.

Examiner

Kenneth B. Wells

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2003.
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-10, 13-20 and 24-28 is/are rejected.
7) ☒ Claim(s) 11, 12 and 21-23 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 26 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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1. Claims 10 and 16 are objected to because of the following informalities: "a transistor driving circuit" lacks clear antecedent basis in claim 10 because it is unclear if this is referring to the same driving circuit set forth in claim 8, or if it is a different driving circuit. In claim 16, line 4, "by" should be deleted. Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-7, 16, 18-20 and 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

As to claims 1-3, note Fig. 3, where the recited "data node" reads on the node where V_i is input; the recited "pass transistor" reads on FET 310; the recited "data pad" reads on either terminal N1 or the terminal where differential signal V_o , $/V_o$ is output; and the recited "driving circuit" reads on all of the circuitry of Fig. 3 other than FET 310 (note that if the data pad is interpreted as the terminal where differential

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signal V_o , $/V_o$ is output, the driving circuit is just the combination of FETs 312 and 314).

As to claims 5 and 6, the first and second power supply voltages are V_{pp} and V_{dd} ; the voltage sensor is the combination of FET 316 and inverters 330, 332; and the control circuit is the combination of FETs 312 and 314.

The "data generator" of claim 16 is the unillustrated circuitry which outputs signal V_i .

The threshold level detector of claim 19 reads on the combination of FET 316 and inverters 330, 332.

The operation recited in claims 7, 20 and 24-28 is seen to be inherent in the Fig. 3 circuitry of Huang et al.

4. Claims 1-4, 8, 16-18, 20 and 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu et al.

As to claims 1-4, note Fig. 4, where the recited "data node" reads on the node S; the recited "pass transistor" reads on FET 36; the recited "data pad" reads on pad 30; and the recited "driving circuit" reads on feedback circuit 31.

As to claim 8, the pull-up and pull-down circuits read on FETs 33 and 34, respectively; and the recited data input terminal is the unillustrated input to driver 32.

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The "data generator" of claim 16 is the combination of FETs 33 and 34.

The operation recited in claims 20 and 24-28 is seen to be inherent in the Fig. 3 circuitry of Huang et al.

5. Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Baek.

Note Fig. 3, where the recited data input terminal reads on the terminal where "DATA" is input; the recited pull-up and pull-down circuits are inherent in the NOR gate 102 (well-known in the art); the recited data node reads on the output terminal of NOR gate 102; the recited pass transistor reads on FET T2; and the recited driving circuit reads on the combination of NOR gate 107, buffer 110 and FET 112. The recited "data pad" reads on the node connected to the drain of FET 106.

As to claim 9, the first and second serially coupled pull-up transistors are well-known components of a NOR gate such as gate 102 of Baek.

The transistor driving circuit of claim 10 reads on the unillustrated circuitry which supplies signal DATA.

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6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al.

The only difference between claim 13 and Huang et al is the recitation of a pull-up and pull-down circuit coupled to the data input terminal and forming the data node therebetween. This would have been obvious, however, to those having ordinary skill in the art who will easily recognize that a well-known inverter can be used to provide signal Vi (the motivation being to either invert or buffer the signal from the circuitry providing Vi). Using such an inverter to provide signal Vi in Huang et al's Fig. 3 will form a circuit reading on instant claim 13.

The operation recited in claims 14 and 15 is seen to be inherent in the Fig. 3 circuitry of Huang et al.

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7. Claims 11, 12 and 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

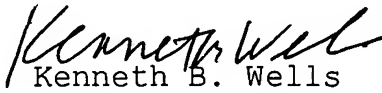
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

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Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Kenneth B. Wells
Primary Examiner
Art Unit 2816

May 28, 2004